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(54) Compact semiconductor device with moulded body

(57) A semiconductor device comprising an insulating film substrate (1) having a surface carrying a high frequency semiconductor chip (2) and other circuit elements (3a to 3e) connected to said semiconductor chip (2), wherein said insulating film substrate (1) is bent a B and laminated, and it is moulded with resin (8) to produce a miniaturized package. A metal layer (5b) acts as an electromagnetic shield. The semiconductor chip (2), which operates at microwave frequencies, receives a spacer layer (7) of a lower dielectric constant than that of the moulding resin (8). In other arrangements, the insulating film is folded in a meandering manner or coiled in the shape of a whirlpool. Alternatively more than one insulating film may be used to carry components and connected together before moulding.

Fig.1

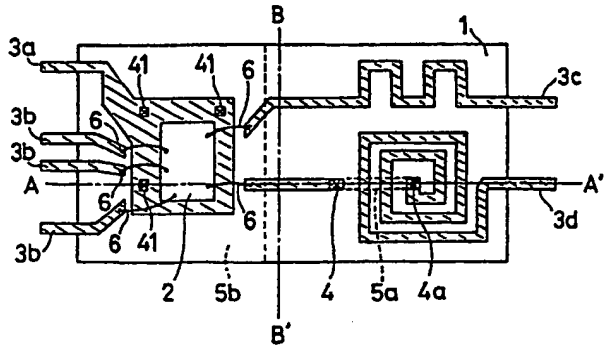

Fig.3

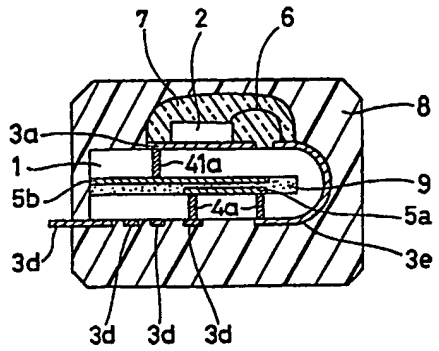

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Fig. 1

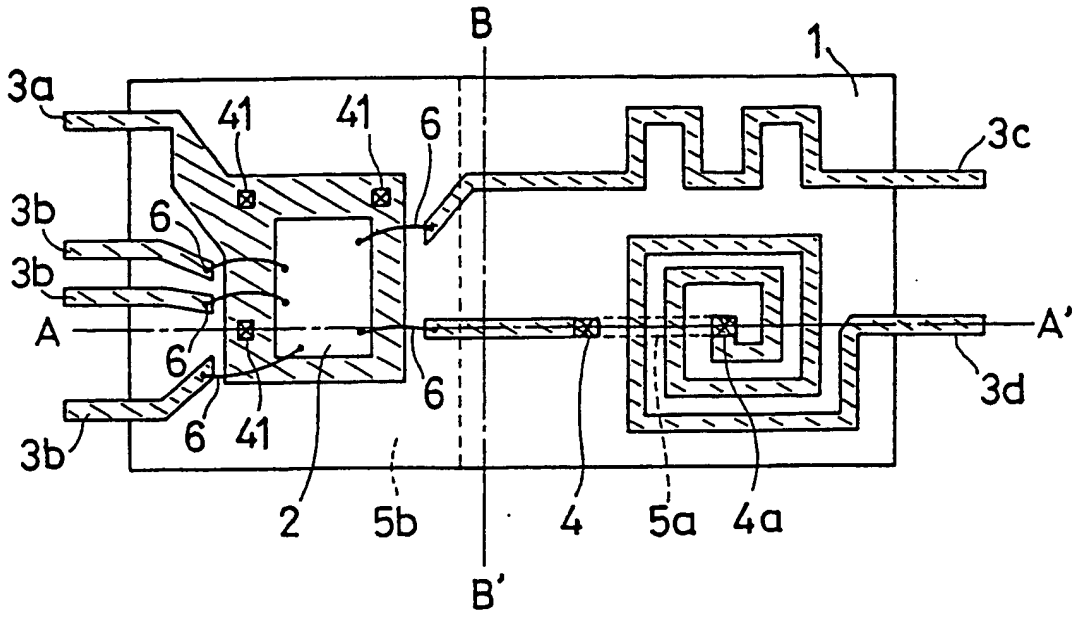

B
1
3a
41
41
6
3c
3b
6
3b
A
A'
6
6
3d
6
41
3b
2
5b
4
5a
4a
B'

Fig. 2

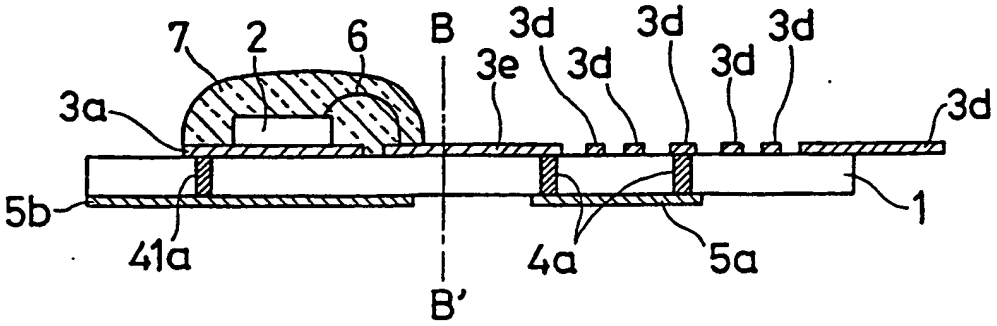

7
2
6
B
3d
3d
3d
3e
3d
3d
3d
3a
3d
5b
1
41a
4a
5a
B'

Fig.3

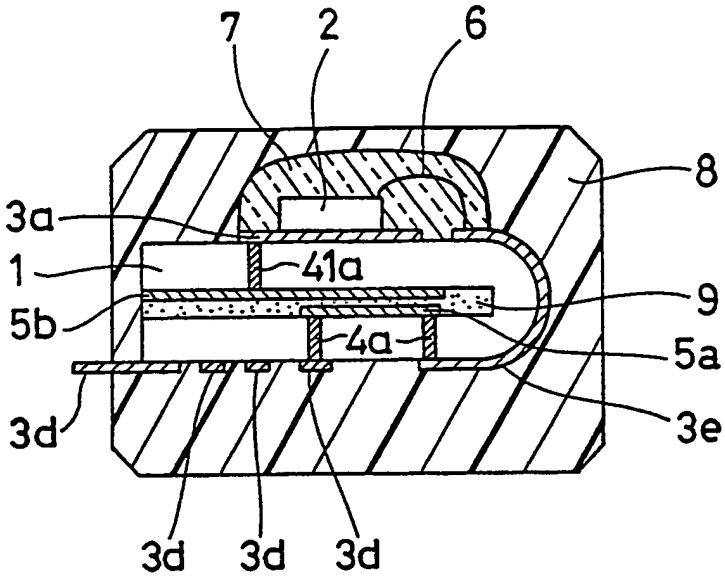


Fig.4

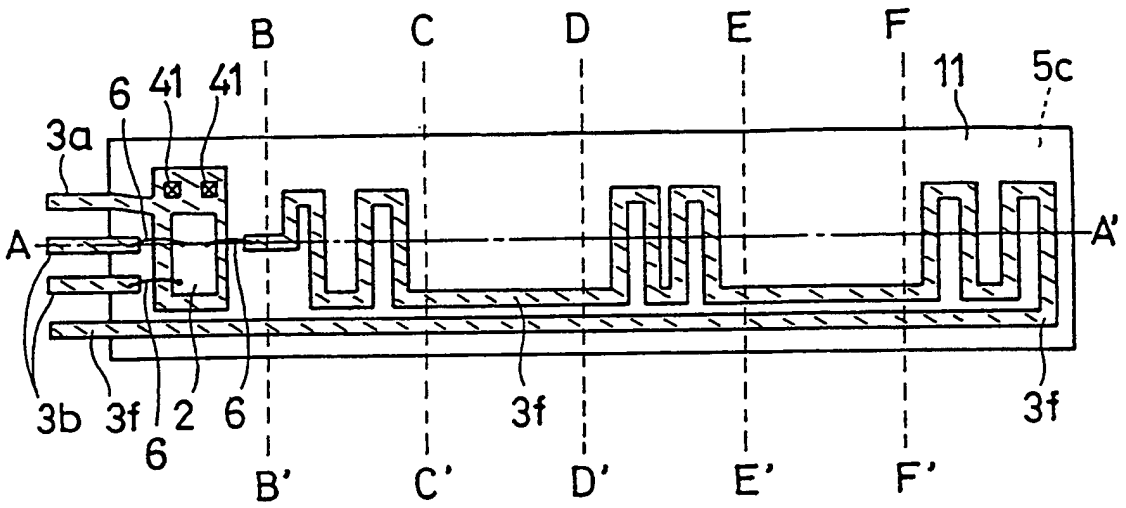

B
C
D
E
F
11
5c
6
41
41
3a
A
A'
3b
3f
2
6
6
3f
3f
B'
C'
D'
E'
F'

Fig.5

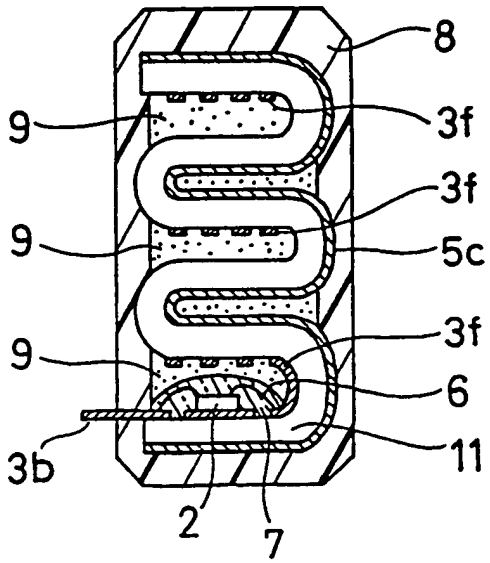

8
9
3f
3f
9
5c
3f
9
6
3b
11
2
7

Fig. 6

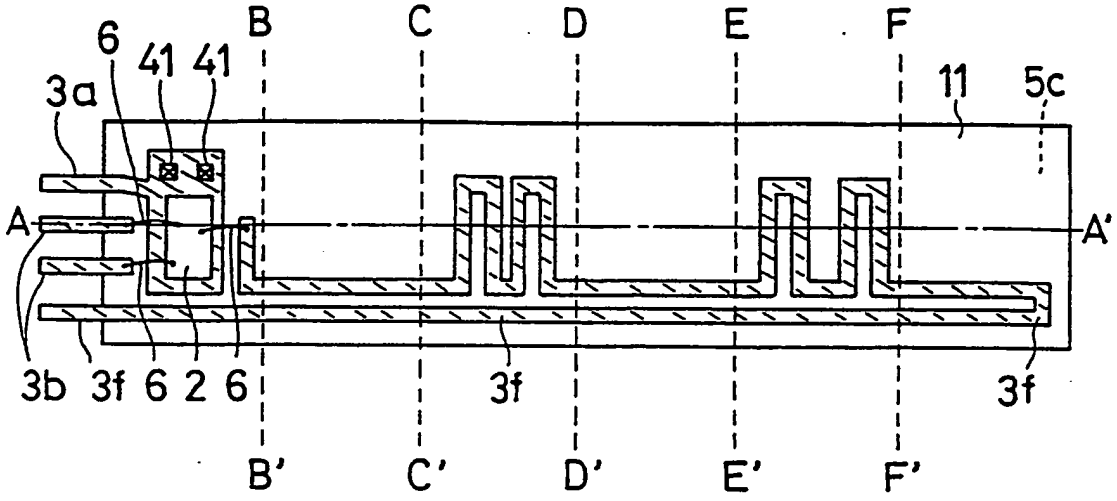

6
41
41
B
C
D
E
F
11
5c
3a
A
A'
3b
3f
6
2
6
3f
3f
B'
C'
D'
E'
F'

Fig. 7

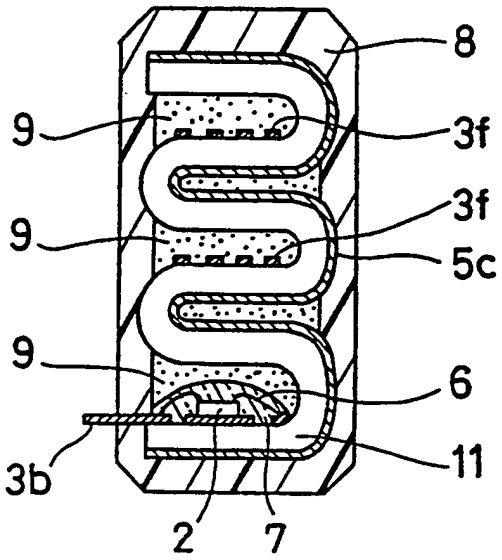

8
9
3f
3f
9
5c
9
6
11
3b
2
7

Fig. 8

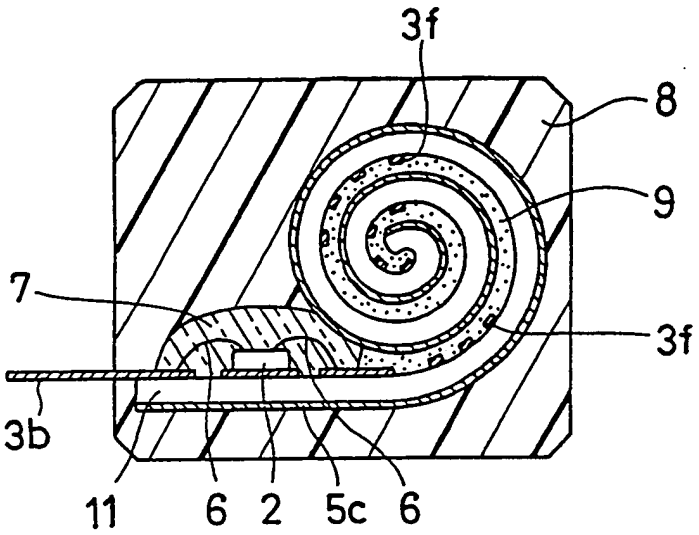


Fig. 9

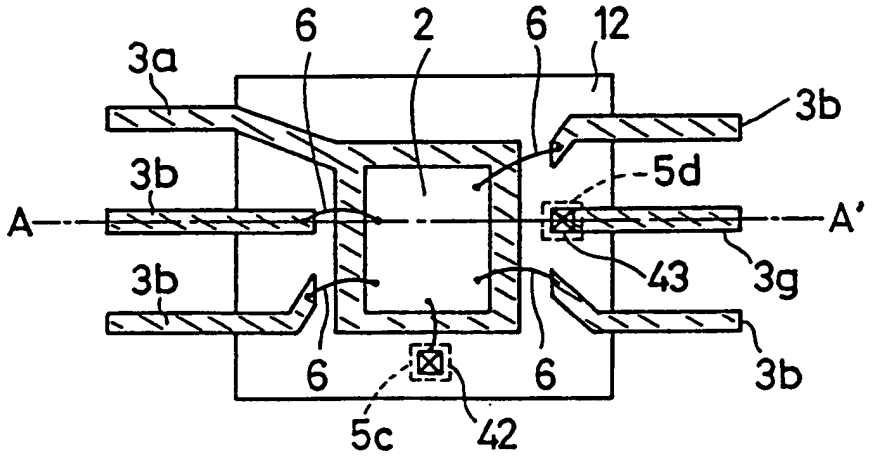


Fig. 10

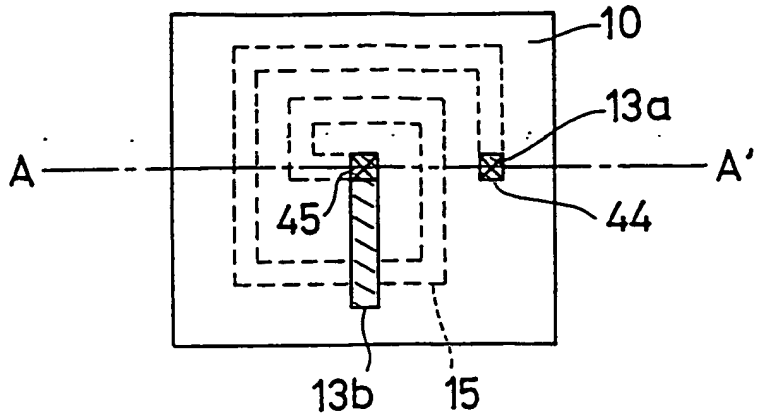

10
13a
A
A'
45
44
13b
15

Fig. 11

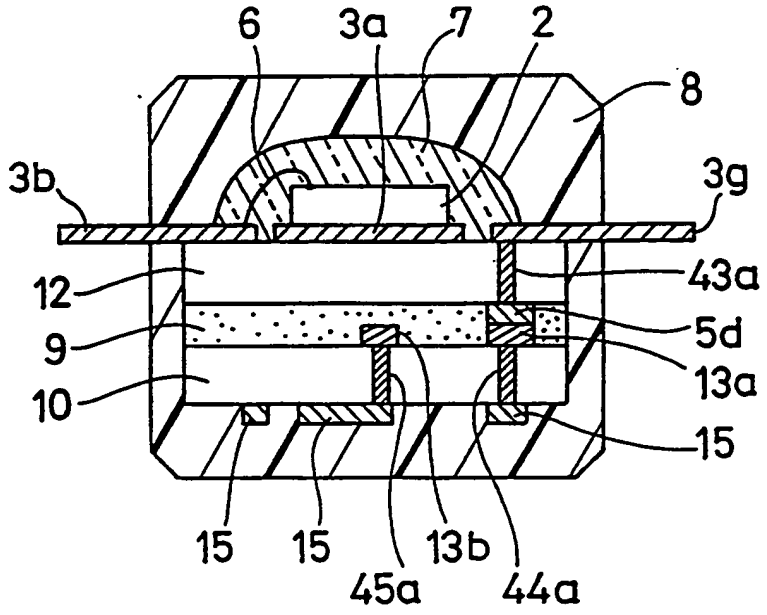

6
3a
7
2
8
3b
3g
12
43a
9
5d
13a
10
15
15
15
13b
45a
44a

Fig.12

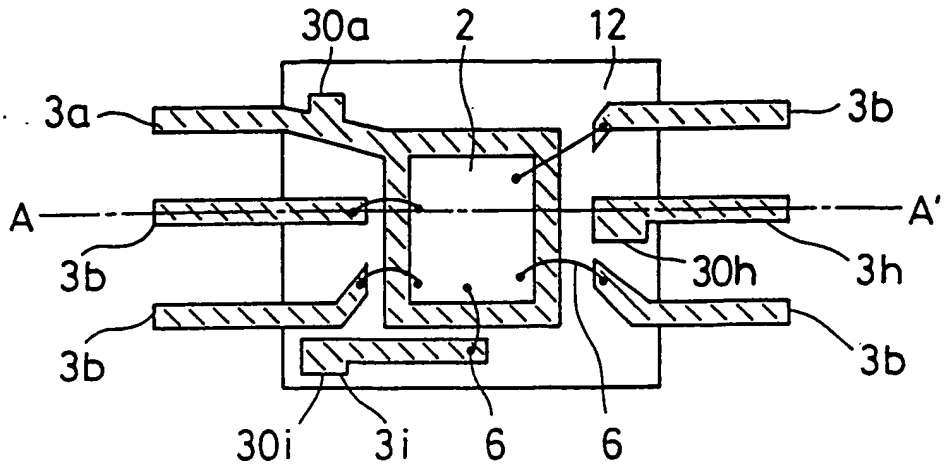

30a
2
12
3a
3b
A
A'
3b
30h
3h
3b
3b
30i
3i
6
6

Fig.13

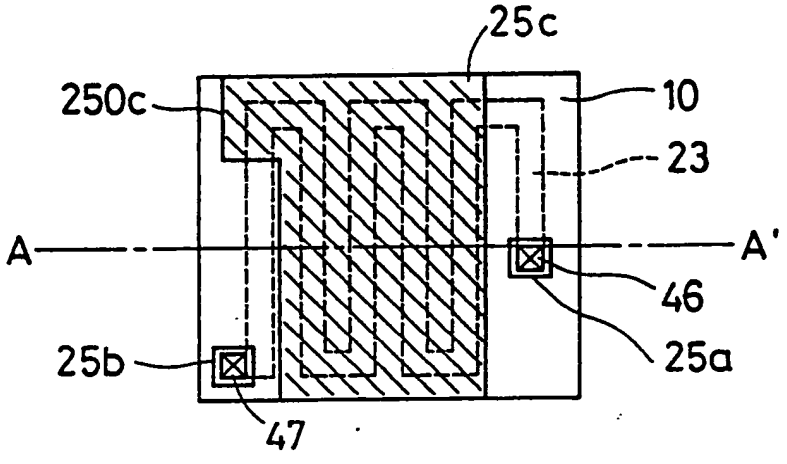

25c
250c
10
23
A
A'
46
25a
25b
47

Fig.14

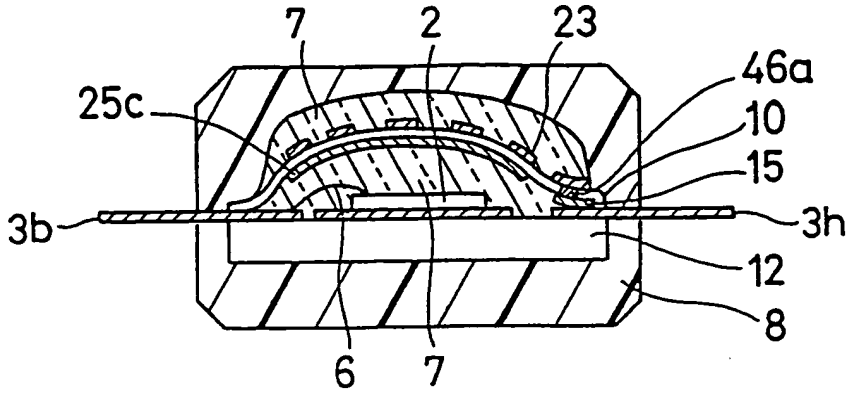

7
2
23
46a
25c
10
15
3b
3h
12
8
6
7

Fig.15

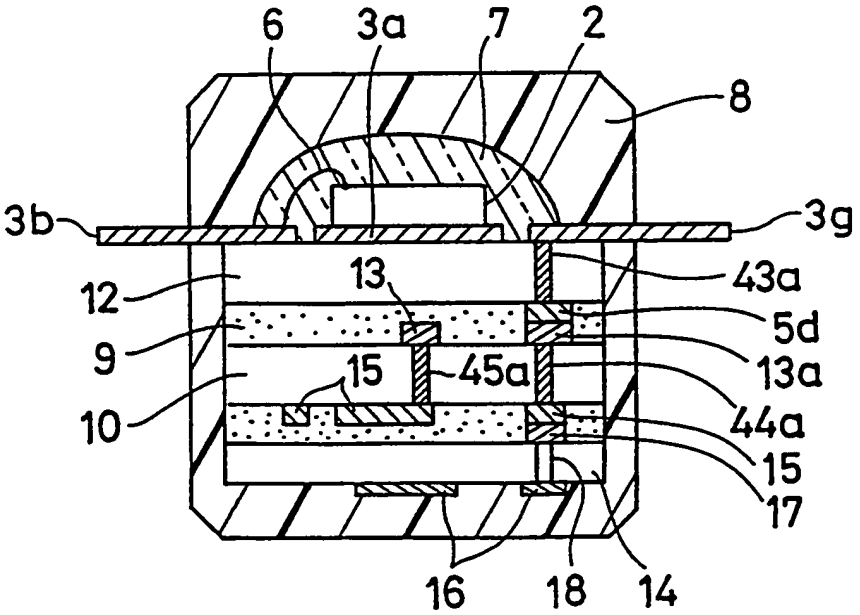

6
3a
7
2
8
3b
3g
13
43a
12
5d
9
15
45a
13a
10
44a
15
17
16
18
14

Fig. 16 (Prior Art)

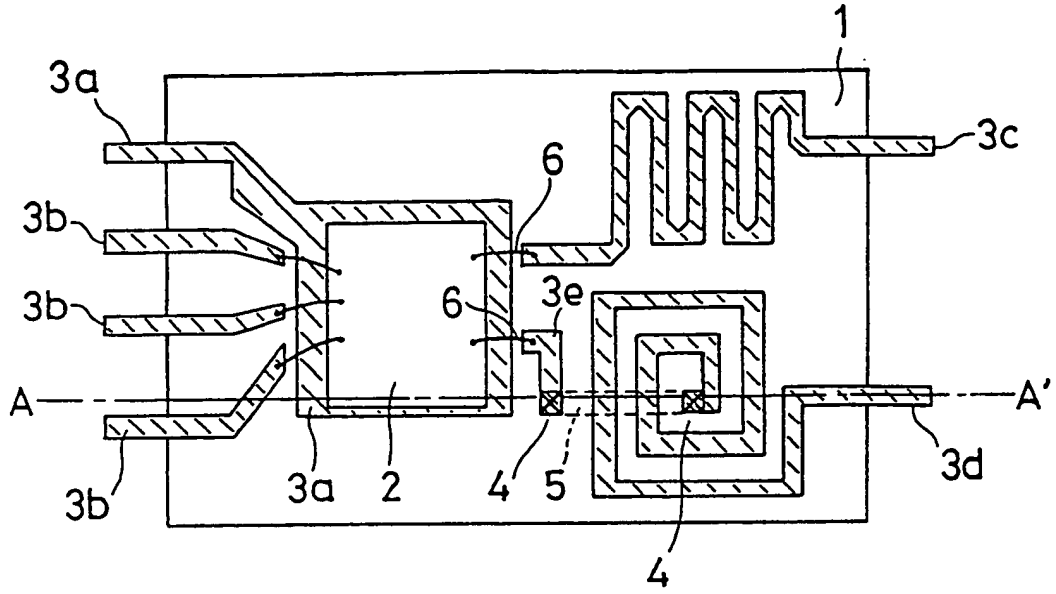
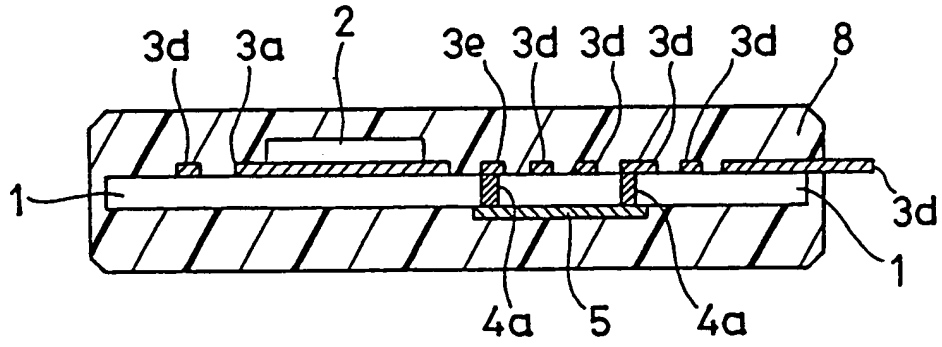


Fig. 17 (Prior Art)



SEMICONDUCTOR DEVICE

FIELD OF THE INVENTION

The present invention relates to a semiconductor device and, more particularly, to a high frequency package for use in microwave band.

BACKGROUND OF THE INVENTIONS

Figure 16 is a top plan view showing a film substrate of a prior art semiconductor device before molding. In the figure, reference numeral 1 designates an insulating film substrate, comprising, for example, polyimide having a thickness of 100 microns and dimensions of 6mm X 8mm, and numeral 2 designates a semiconductor chip for use at high frequencies, for example, an amplifier which is several millimeters along each edge. Numerals 3a to 3e designate upper metal wiring patterns having a thickness of approximately 10 microns which are formed on the insulating film substrate 1, generally with metal such as cover on the same surface, numeral 3a designates a grounding pad of the high frequency semiconductor chip 2, numeral 3b designates an external lead for exchanging signals with the high frequency semiconductor chip 2, numeral 3c designates a meandering type inductor for adjusting inductance when bias voltage is applied to the high frequency semiconductor chip 2, numeral 3d designates a spiral type inductor similarly for adjusting inductance when bias voltage is applied to the

high frequency semiconductor chip 2, and numeral 3e designates an auxiliary wiring connected to the spiral type inductor 3d via a through hole described below. The upper metal wiring patterns 3b to 3d are respectively connected to the high frequency semiconductor chip 2 by wirings 6 of gold or the like. Numeral 4 designates a through hole formed in the insulating film substrate 1 for electrically connecting a lower metal wiring pattern 5 formed on the rear surface of the film substrate 1 to the upper metal wiring patterns 3 via a conductive material filled in the through hole 4, where an end part of the spiral type inductor 3d is connected to the auxiliary wiring 3e via the through holes 4 and the lower metal wiring pattern 5.

Figure 17 is a cross section taken along a line A-A' of Figure 16 showing a semiconductor device after molding. In the figure, numeral 8 designates a molding material for which resin is generally employed. Generally, the high frequency semiconductor chip 2 and the upper metal wiring pattern (grounding pad) 3a are die-bonded with solder or the like. A grounding conductive layer (which is not shown in the figure) on the rear surface of the high frequency semiconductor chip 2 is electrically connected to the upper metal wiring pattern (grounding pad) 3a. Further, numeral 4a designates a conductive material filled in the through hole 4.

Next, description is given of the operations.

In a semiconductor device operating at high frequencies such as microwave band, in general, since wirings serve as a distributed constant line, the wirings themselves operate as a passive circuit. Further, since the device operates at high frequencies, an inductor of minute inductance (approximately several nH) is often employed. In other words, the upper metal wiring patterns 3c and 3d on the film substrate 1 in Figure 16 respectively serve as the meandering type inductor and the spiral type inductor, when bias voltage is applied to the high frequency semiconductor chip 2 which is the amplifier. Since a passive circuit by wirings is generally large-sized as illustrated in Figure 16, a package which is obtained by molding this passive circuit is also large-sized.

As the prior art device is constructed as described above, the package is unfavorably oversized, resulting in obstacle to minimization of a system including the package.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a semiconductor device in which a package size is miniaturized with the same functions as the prior art device without deteriorating high frequency characteristics.

Other objects and advantages of the present invention will become apparent from the detailed description given

hereinafter; it should be understood, however, that the detailed description and specific embodiment are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to the those skilled in the art from this detailed description.

In a semiconductor device in accordance with the present invention, the molding is conducted in a state where an insulating film substrate is bent and piled up, an insulating film substrate is bent several times and laminated or an insulating film substrate is rolled up in whirlpool shape. This provides a miniaturized package. By disposing an electromagnetic shielding layer between the laminated surfaces of the film substrate, coupling of high frequency signals between the neighboring surfaces of the film substrate is prevented, providing a package with less deterioration of high frequency characteristics.

Since a plurality of insulating film substrates are employed, the second film substrate adheres to the surface of the first film substrate opposite to the surface, on which a semiconductor chip is formed, and the semiconductor chip on the first film substrate is electrically connected to circuit elements on the second film substrate, or since molding is conducted in a state where the second film substrate is laminated and adheres to the first film

substrate having the semiconductor chip covered with an insulating spacer material, and the semiconductor chip on the first film substrate is connected to the circuit elements on the second film substrate, the circuit is disposed in three dimensions, providing a miniaturized package.

When the second film substrate is laminated on the first film substrate, since an electromagnetic shielding layer is disposed on the second film substrate to cover the semiconductor chip on the first film substrate, radiation of electromagnetic wave from the circuit elements on the first film substrate or coupling of high frequency signals with the circuit elements outside the package is prevented, resulting in obtaining a package having high reliability.

By employing a material having a high rigidity for the film substrate mounting the semiconductor chip thereon, among the plural film substrates, a package that is easily fabricated and processed is provided, which package prevents bending stress added to the semiconductor chip, hardly generating destruction of the chip.

By covering the semiconductor chip or the circuit elements with a material having a dielectric constant lower than a molding material, parasitic capacitances over circuit elements such as the semiconductor chip or metal wiring patterns are reduced, providing a package having less

deterioration in high frequency characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a top plan view showing an insulating film substrate of a semiconductor device before molding in accordance with a first embodiment of the present invention.

Figure 2 is a cross sectional view showing the insulating film substrate of Figure 1 after covering a semiconductor chip with spacer material.

Figure 3 is a cross sectional view showing the semiconductor device in which the semiconductor chip is covered with spacer material and the whole of the insulating film substrate is molded.

Figure 4 is a top plan view showing an insulating film substrate of a semiconductor device before molding in accordance with a second embodiment of the present invention.

Figure 5 is a cross sectional view showing the semiconductor device in which the insulating film substrate of Figure 4 is molded.

Figure 6 is a top plan view showing an insulating film substrate before molding in accordance with a variation of the second embodiment of the present invention.

Figure 7 is a cross sectional view showing the semiconductor device in which the insulating film substrate of Figure 6 is molded.

Figure 8 is a cross sectional view showing a semiconductor device in accordance with a third embodiment of the present invention.

Figure 9 is a top plan view showing a first film substrate before molding in accordance with a fourth embodiment of the present invention.

Figure 10 is a top plan view showing a second film substrate before molding in accordance with the fourth embodiment of the present invention.

Figure 11 is a cross sectional view showing a semiconductor device in which the first and the second film substrates are molded in the fourth embodiment.

Figure 12 is a top plan view showing a first film substrate before molding in accordance with a fifth embodiment of the present invention.

Figure 13 is a top plan view showing a second film substrate before molding in accordance with the fifth embodiment of the present invention.

Figure 14 is a cross sectional view showing a semiconductor device in which the first and the second film substrates are molded in the fifth embodiment.

Figure 15 is a cross sectional view showing a semiconductor in which three film substrates are laminated in accordance with the fourth embodiment of the present invention.

Figure 16 is a top plan view showing a film substrate of a prior art semiconductor device before molding.

Figure 17 is a sectional view showing the prior art semiconductor device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Embodiments of the present invention will be described in detail with reference to the drawings.

Figure 1 is a top plan view showing a semiconductor device before molding in accordance with a first embodiment of the present invention. In the figure, the same reference numerals as those of Figure 16 designate the same or corresponding parts. Through holes 41 are formed on the insulating film substrate 1, for example, having a thickness of 100 microns and dimensions of 6mm X 8mm, so as to connect the grounding pad 3a mounting the high frequency semiconductor chip 2 thereon to a lower metal wiring pattern 5b, in which a conductive material 41a is filled. A line B-B' shows a bending position when the film substrate 1 is bent such that a lower metal wiring pattern 5a is opposite to the lower metal wiring pattern 5b.

Figure 2 is a cross section taken along a line A-A' of Figure 1 showing a semiconductor device in which surroundings of the semiconductor chip 2 before molding are covered with spacer material 7 having a low dielectric constant and high insulating property such as glass.

Figure 3 is a cross section showing a semiconductor device in which the film substrate 1 shown in Figure 2 is bent at a line B-B' and molded. Reference numeral 8 designates such molding material as resin. An insulating adhesive 9 is coated in the space sandwiched by the rear surfaces of the bent film substrate 1.

Next, a description is given of a production method therefor.

Two methods for producing a semiconductor device illustrated in Figure 3 will be described below.

(1) After die-bonding the semiconductor chip 2 on the film substrate 1 and bonding the chip 2 by wirings 6, the film substrate 1 is bent along a line B-B' and molded.

(2) After bending the film substrate 1 along a line B-B' in advance, the semiconductor chip 2 is die-bonded, bonded by wirings 6, and molded.

The spacer material 7 may be produced at any time after bonding. Even in the method (1), it is possible to prevent bending stress from acting upon the spacer material 7 in bending the film substrate 1, by designing such that a length of the film substrate 1 in the longitudinal direction in the vicinity of the bending position B-B' is several times as long as a thickness of the film substrate 1.

A description is given of the functions and the effects.

In this package, by bending the film substrate 1 at the bending position of a line B-B' of Figure 1 and disposing the meandering type inductor 3c or the spiral type inductor 3d which is provided in the right side of the bending position of a line B-B' in the figure below the semiconductor chip 2, it is possible to dispose a circuit in three dimensions, resulting in miniaturization of the package.

By combining the upper metal wiring pattern (grounding pad) 3a connected to a grounding conductive layer on the rear surface of the semiconductor chip 2 by solder or the like, with the lower metal wiring pattern 5b via the through hole 41, the lower metal wiring pattern 5b serves as an electromagnetic shielding layer. As a result, it is possible to shield an electromagnetic field which cannot be enough shielded by the grounding pad 3a, to prevent signals influencing with each other between neighboring signal lines, namely, so-called coupling, and to isolate electrically the semiconductor chip 2 from the inductors 3c and 3d, resulting in no deterioration of high frequency characteristics.

Still, by covering over the semiconductor chip 2 with the spacer material 7 having a dielectric constant lower than the molding material 8, parasitic capacitances of the molding material 8 can be reduced, resulting in reducing

miniaturize a package to a greater extent than a case where the film substrate is just folded in two as described in the first embodiment. Further, in this structure, by turning the film substrate 1 several times, it is possible to prevent coupling between neighboring units produced by the film substrate turned in U-shape, each unit separated by the lower metal wiring pattern 5c, while coupling occurs between the confronting film surfaces on one of which the semiconductor chip 2 is formed. In addition, by forming the meandering type inductor 3f shifted so as not to be opposite to the semiconductor chip 2, as illustrated in Figure 6, and constructing the semiconductor device with the film turned several times, as illustrated in Figure 7, coupling between the opposite upper and lower surfaces can be prevented, too. Here, while the insulating adhesive 9 is also coated in intervals sandwiched by the bent film substrate in this embodiment, the insulating adhesive 9 is not required when there is no problem about short-circuiting.

Figure 8 is a cross sectional view showing a semiconductor device in accordance with a third embodiment of the present invention. As illustrated in the figure, in this embodiment, by rolling the film substrate 11 including the relatively large size inductor 3f as shown in Figure 4 in whirlpool shape, a circuit is disposed in three dimensions. In order to obtain such structure, the

deterioration of high frequency characteristics due to parasitic capacitances.

In addition, while the insulating adhesive 9 is coated in intervals sandwiched by the bent film substrate 1 in the first embodiment, since the adhesive 9 is coated so as to insulate the metal wiring 5a from the metal wiring 5b rather than to adhere to materials, the insulating adhesive 9 is not required if the metal wirings 5a and 5b can keep a predetermined distance not to short-circuit.

Figure 4 is a top plan view showing a semiconductor device before molding in accordance with a second embodiment of the present invention. As illustrated in the figure, a relatively large meandering type inductor 3f is formed on an insulating film substrate 11 having a size corresponding to the inductor 3f and a lower metal wiring pattern 5c is formed on the whole rear surface, which is connected to the grounding pad 3a via the through hole 41.

Figure 5 is a cross section taken along a line A-A' of Figure 4 showing a semiconductor device in which the insulating film substrate 11 is bent at the respective parts, B-B', C-C', D-D', E-E' and F-F' like bellows shape in cross-section and is molded. Thus, by bending the film substrate 11 several times, a circuit with a plurality of layers is disposed in three dimensions. As a result, in dealing with a long film substrate, it is possible to

insulating adhesive 9 may be coated on the whole surface of the region of the film substrate 11 of Figure 4 on which the inductor 3f is formed and the film substrate 11 be lefthandedly rolled up from an end opposite to the other end mounting the semiconductor chip 2 thereon. As a result, a package is miniaturized. Also, due to the lower metal wiring pattern 5c intervening between the neighboring portions of the film substrate, it is possible to reduce coupling of high frequency signals which may occur in the circuit constructed in three dimensions, resulting in no deterioration of high frequency characteristics.

Figure 9 is a top plan view showing a first film substrate 12 on which the semiconductor chip before molding is mounted in accordance with a fourth embodiment of the present invention. Figure 10 is a top plan view showing a second film substrate 10 on which a spiral type inductor is formed. In this embodiment, as illustrated in Figure 11, with employing two film substrates and forming a circuit on each film substrate, molding is conducted with these film substrates laminated.

More particularly, in the figures, the semiconductor chip 2 is die-bonded with the grounding pad 3a formed on the top surface of the first film substrate 12, and the chip 2 is connected to the external lead 3b by wiring 6 and connected to the lower metal wiring pattern 5c via a through

hole 42. An upper metal wiring pattern 3g for applying bias voltage to the inductor is formed on the top surface of the first film substrate 12, which is connected to a lower metal wiring pattern 5d via a through hole 43. Here, the lower metal wiring patterns 5c and 5d serve as a connecting pad. On the rear surface of the second film substrate 10, a spiral type inductor is formed by a lower metal wiring pattern 15 and both end parts thereof are respectively connected to the upper metal wiring patterns 13a and 13b via through holes 44 and 45. Here, the upper metal wiring pattern 13a serves as a connecting pad with the lower metal wiring pattern 5d provided on the rear surface of the first film substrate 12. The upper metal wiring pattern 13b serves as an auxiliary wiring for connecting with the lower metal wiring pattern 5c provided on the rear surface of the first film substrate 12.

In the first film substrate 12 constructed as described above, the semiconductor chip 2 is covered with the spacer material 7 after wire-bonding. And, as illustrated in Figure 11, the rear surface of the first film substrate 12 is opposite to the top surface of the second film substrate 10, the insulating adhesive 9 is coated between these film substrates, and the lower metal wiring patterns 5c and 5d on the rear surface of the first film substrate 12, are contacted, respectively, with upper metal wiring patterns

13b and 13a on the top surface of the second film substrate 10. Next, in this state, molding is carried out with the molding material 8. Here, reference numerals 43a, 44a and 45a designate conductive materials filled, respectively, in the through holes 43, 44 and 45.

As constructed as described above, since the spiral type inductor 15 is disposed in three dimensions under the semiconductor chip 2, the package is diminished in size. Further, in this embodiment, since only the semiconductor chip 2 is mounted on the first film substrate 12, it is possible to prevent coupling of high frequency signals between the semiconductor chip 2 and the spiral type inductor comprising the metal wiring 15, by the grounding pad 3a connected to the grounding electrode on the rear surface of the semiconductor chip 2, resulting in no deterioration of high frequency characteristics. In addition, in this embodiment, since the semiconductor chip 2 is covered with the spacer material 7 having a dielectric constant lower than the molding material 8, it is possible to suppress generating unnecessary parasitic capacitances, resulting in forming a package having improved high frequency characteristics. Further, by employing material such as ceramic for the first film substrate 12, which is harder than the second film substrate 10, the second film substrate 10 is bent and the first and the second film

substrates 12 and 10 are laminated, preventing damages by bending of the semiconductor chip 2, due to thermal deformation of resin 7 in molding. In addition, even if difference arise in intervals between the film substrates depending on the coated state of the insulating adhesive 9, the underlying film substrate 10 is deformed because the film substrate 12 has higher rigidity than the film substrate 10, thereby the lower metal wiring patterns 5c and 5d are kept in contact with the upper metal wiring patterns 13b and 13a, resulting in easily processing and fabricating a package.

Figure 12 is a top plan view showing the first film substrate 12 before molding in accordance with a fifth embodiment of the present invention. Figure 13 is a top plan view showing the second film substrate 10 on which a spiral type inductor is formed. In this embodiment, the film substrate on which the inductor is formed is laminated on the film substrate on which the semiconductor chip is mounted. In the figures, the semiconductor chip 2 is die-bonded on the top surface of the first film substrate 12 via the grounding pad 3a, the semiconductor chip 2 is connected to the external leads 3b by the wirings 6, upper metal wiring patterns 3h and 3i are formed for connecting to upper metal wiring patterns on the second film substrate, and the upper metal wiring pattern 3i is connected to the semiconductor chip 2 by the wiring 6. Further, in order to

easily connect to upper metal wiring patterns on the second film substrate, addition parts 30a, 30h and 30i are respectively attached to the upper metal wiring patterns 3a, 3h and 3i. On the rear surface of the second film substrate 10, a meandering type inductor is formed by a lower metal wiring pattern 23 and both end parts thereof are respectively connected to upper metal wiring patterns 25a and 25b via through holes 46 and 47. In addition, an upper metal wiring pattern 25c is formed on the surface of the second film substrate 10, in a relatively large region excepting the region where the lower metal wiring patterns 25a and 25b are provided, to become an electromagnetic shielding layer. Further, an addition part 250c is attached to this upper metal wiring pattern 25c, in order to easily connect to the addition part 30a of the grounding pad 3a on the first film substrate 12. Here, the upper metal wiring patterns 25a and 25b on the second film substrate 10 serve as connecting pads with the addition parts 30h and 30i of the upper metal wiring patterns 3h and 3i on the first film substrate 12.

In the first film substrate 12 constructed as described above, the semiconductor chip 2 is covered with the spacer material 7 after wire-bonding. And, as illustrated in Figure 14, the top surface of the first film substrate 12 is opposite to the top surface of the second film substrate 10,

the spacer material 7 intervenes between these film substrates, and the upper metal wiring patterns 25a and 25b and the addition part 250c on the surface of the second film substrate 10, are contacted, respectively, with upper metal wiring patterns 3h and 3i and the addition part 30a on the top surface of the first film substrate 12. In addition, the rear surface of the second film substrate 10 is covered with the spacer material 7. Next, in this state, molding is carried out with the molding material 8. Here, reference numeral 46a designates a conductive material filled in the through hole 46.

As constructed as described above, since the inductor 23 is disposed in three dimensions over the semiconductor chip 2, the package is diminished in size. In addition, as described above, since the upper metal wiring pattern 25c to be an electromagnetic shielding layer is disposed between the semiconductor chip 2 and the inductor 23 of the film substrate 10, the coupling of high frequency signals between the film substrates can be reduced, resulting in no deterioration of high frequency characteristics. Further, since the upper metal wiring pattern 25c is disposed to cover the semiconductor chip 2, it is possible to reduce leakage of high frequency electromagnetic wave from the semiconductor chip 2 to the outside of the package, resulting in so-called high frequency shielding. Further,

in this fifth embodiment, by employing a harder material than the second film substrate 10 for the first film substrate 12, even if stress is added to the first film substrate 12 by bending the second film substrate 10 in molding, the semiconductor chip 2 is kept level and the chip 2 does not receive damages, resulting in improved assembling property and processing property. Since a material having a lower dielectric constant than the molding material 8 is employed for the spacer material 7 between the first film substrate 12 and the second film substrate 10 and the spacer material 7 on the lower metal pattern 23 of the second film substrate 10, unnecessary parasitic capacitances can be reduced. Further, in the fifth embodiment, a lower metal wiring pattern may be formed on the rear surface of the first film substrate 12 and this wiring pattern may be connected to the upper metal wiring patterns via through holes.

While, in the above-described embodiments, the spiral type and/or the meandering type inductor is shown for a circuit element, which is constructed with the upper and/or the lower metal wiring pattern of the insulating film substrate, a stub for matching impedance, a resonance circuit or the like may be constructed with wiring patterns.

The times of bending the film substrate in the second embodiment, the times of rolling the film substrate in the

third embodiment and the times of piling up the film substrates in the fourth and the fifth embodiments are not limited thereto. For example, as illustrated in Figure 15, by disposing a third film substrate 14 having an upper metal wiring pattern 17 and a lower metal wiring pattern 16 mutually connected via a through hole conductive material 18 under the second film substrate 10 and connecting the film substrate 14 to a lower metal wiring pattern 15 on the second film substrate 10 by the upper metal wiring pattern 17, a semiconductor device having a structure of three laminated film substrates can be obtained.

Still, while the insulating adhesive 9 is coated between the film substrates in the second to the fifth embodiments, since the adhesive 9 is coated so as to insulate rather than to adhere to materials, the adhesive 9 is not required without possibility of short-circuiting.

As described above, in a semiconductor device in accordance with the present invention, the molding is conducted in a state where an insulating film substrate is bent and piled up, an insulating film substrate is bent several times and laminated or an insulating film substrate is rolled up in whirlpool shape. This provides a miniaturized package. By disposing an electromagnetic shielding layer between the laminated surfaces of the film substrate, coupling of high frequency signals between the

neighboring surfaces of the film substrate is prevented, providing a package with less deterioration of high frequency characteristics.

Since a plurality of insulating film substrates are employed, the second film substrate adheres to the surface of the first film substrate opposite to the surface on which a semiconductor chip is formed, and the semiconductor chip on the first film substrate is electrically connected to circuit elements on the second film substrate, or since molding is conducted in a state where the second film substrate is laminated and adheres to the first film substrate having the semiconductor chip covered with an insulating spacer material and the semiconductor chip on the first film substrate is connected to the circuit elements on the second film substrate, the circuit is disposed in three dimensions, resulting in a miniaturized package.

When the second film substrate is laminated on the first film substrate, since an electromagnetic shielding layer is disposed on the second film substrate to cover the semiconductor chip on the first film substrate, radiation of electromagnetic wave from the circuit elements on the first film substrate or coupling of high frequency signals with the circuit elements outside the package is prevented, resulting in obtaining a package having high reliability.

By employing a material having a high rigidity for the

film substrate mounting the semiconductor chip thereon, among the plural film substrates, a package that is easily fabricated and processed is provided, which package prevents bending stress added to the semiconductor chip, hardly generating destruction of the chip.

By covering the semiconductor chip or the circuit elements with a material having a dielectric constant lower than a molding material, parasitic capacitances over circuit elements such as the semiconductor chip or metal wiring patterns are reduced, providing in a package having less deterioration in high frequency characteristics.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising an insulating film substrate (1) having a surface, a high frequency semiconductor chip (2) disposed on said surface and circuit elements (3a to 3e) disposed on said surface and connected to said semiconductor chip (2), wherein said insulating film substrate (1) is bent and laminated, and it is molded with resin (8).

2. The semiconductor device of Claim 1, wherein said insulating film substrate (1) is bent with positioning its rear surface inside with making upper and lower surfaces opposite to each other.

3. The semiconductor device of Claim 2, further comprising an electromagnetic shielding layer (5b) on said upper surface for separating electromagnetically said upper surface from said lower surface.

4. A semiconductor device comprising an insulating film substrate (11) having a surface, a high frequency semiconductor chip (2) disposed on said surface and circuit elements (3a, 3b, 3f) disposed on said surface and connected to said semiconductor chip (2), wherein said insulating film

substrate (11) is folded several times with overlapping with each other, like bellows shape in cross-section, with making several sets of opposite portions of said surface, and it is molded with resin (8).

5. The semiconductor device of Claim 4, wherein said semiconductor chip (2) and/or said circuit elements (3a, 3b, 3f) are disposed on either of the opposite portions of said surface of said film substrate (11).

6. The semiconductor device of Claim 4, further comprising an electromagnetic shielding layer (5c) disposed on the whole surface of said insulating film substrate (11).

7. A semiconductor device comprising an insulating film substrate (11) having a surface, a high frequency semiconductor chip (2) disposed on said surface and circuit elements (3a, 3b, 3f) disposed on said surface and connected to said semiconductor chip (2), wherein said insulating film substrate (11) is rolled up in whirlpool shape from its on end and it is molded with resin (8).

8. The semiconductor device of Claim 7, wherein said one end of said insulating film substrate (11) is rolled in with positioning said surface inside.

9. The semiconductor device of Claim 7, further comprising an electromagnetic shielding layer (5c) disposed on the whole rear surface of said insulating film substrate (11), so that adjacent portions of said film substrate (11), which is rolled up to be laminated, are electromagnetically separated.

10. A semiconductor device comprising a first insulating film substrate (12) having a high frequency semiconductor chip (2) and circuit elements (3a, 3b, 3g) connected to said semiconductor chip (2) disposed on a surface and a second insulating film substrate (10) having a circuit element (15) on a rear surface, wherein said first film substrate (12) and said second film substrate (10) are laminated and mutually electrically connected, and it is molded with resin (8).

11. The semiconductor device of Claim 10, wherein a rear surface of said first film substrate (12) is opposite to a surface of said second film substrate (10) and these two film substrates are mutually electrically connected via through holes (43 to 45).

12. The semiconductor device of Claim 10, wherein said surface of said first film substrate (12) is opposite to a

surface of said second film substrate (10) and these two film substrates are mutually electrically connected via through holes (46, 47).

13. The semiconductor device of Claim 10, wherein said first film substrate (12) is harder than said second film substrate (10).

14. The semiconductor device of Claim 12, further comprising an electromagnetic shielding layer (25c) disposed on said surface of said second film substrate (10) for electromagnetically separating said second film substrate (10) from said first film substrate (12).

15. The semiconductor device of Claim 12, further comprising a circuit element (23), which is formed on said rear surface of said second film substrate (10) and covered with a material (7) having a dielectric constant lower than that of said resin (8).

16. The semiconductor device of Claim 1, wherein said semiconductor chip (2) is covered with a material (7) having a dielectric constant lower than that of said resin (8).

17. The semiconductor device of Claim 4, wherein said

semiconductor chip (2) is covered with a material (7) having a dielectric constant lower than that of said resin (8).

18. The semiconductor device of Claim 7, wherein said semiconductor chip (2) is covered with a material (7) having a dielectric constant lower than that of said resin (8).

19. The semiconductor device of Claim 10, wherein said semiconductor chip (2) is covered with a material (7) having a dielectric constant lower than that of said resin (8).

20. A semiconductor device substantially as hereinbefore described with reference to the five embodiments illustrated in Figures 1 to 15 of the accompanying drawings.

Amendments to the claims have been filed as follows

1. A semiconductor device comprising an insulating film substrate (1) having a surface, said surface possessing an upper layer and a lower layer, and a high frequency semiconductor chip (2) disposed on said surface and circuit elements (3a to 3e) disposed on said surface and connected to said semiconductor chip (2), wherein said insulating film substrate (1) is bent and laminated, and it is molded with resin (8) and said upper surface is separated from said lower surface by an electromagnetic shielding layer (5b).

2. The semiconductor device of claim 1, wherein said insulating film substrate (1) is bent with positioning its rear surface inside with making upper and lower surfaces opposite to each other.

3. A semiconductor device comprising an insulating film substrate (11) having a surface, said surface possessing an upper layer and a lower layer, and a high frequency semiconductor chip (2) disposed on said surface and circuit elements (3a, 3b, 3f) disposed on said surface and connected to said semiconductor chip (2), wherein said insulating film substrate (11) is folded several

times with overlapping with each other, like bellows shape in cross-section, with making several sets of opposite portions of said surface, and it is molded with resin (8) and the whole surface of said insulating film substrate (11) has an electromagnetic shielding layer (5c) disposed thereon.

4. The semiconductor device of claim 3, wherein said semiconductor chip (2) and/or said circuit elements (3a, 3b, 3f) are disposed on either of the opposite portions of said surface of said film substrate (11).

5. A semiconductor device comprising an insulating film substrate (11) having a surface, a high frequency semicondutor chip (2) disposed on said surface and circuit elements (3a, 3b, 3f) disposed on said surface and connected to said semiconductor chip (2), wherein said insulating film substrate (11) is rolled up in whirlpool shape from its one end and it is molded with resin (8).

6. The semiconductor device of claim 5, wherein said one end of said insulating film substrate (11) is rolled in with positioning said surface inside.

7. The semiconductor device of claim 5, further comprising an electromagnetic shielding layer (5c)

disposed on the whole rear surface of said insulating film substrate (11) so that adjacent portions of said film substrate (11), which is rolled up to be laminated, are electromagnetically separated.

8. A semiconductor device comprising a first insulating film substrate (12) having a high frequency semiconductor chip (2) and circuit elements (3a, 3b, 3g) connected to said semiconductor chip (2) disposed on a surface and a second insulating film substrate (10) having a circuit element (15) on a rear surface, wherein said rear surface of said first film substrate (12) is opposite to a surface of said second film substrate (10) and these two film substrates are mutually electrically connected via through holes (43 to 45) and said first film substrate (12) and said second film substrate (10) are laminated and mutually electrically connected, and they are molded with resin (8).

9. A semiconductor device comprising a first insulating film substrate (12) having a high frequency semiconductor chip (2) and circuit elements (3a, 3b, 3g) connected to said semiconductor chip (2) disposed on a surface and a second insulating film substrate (10) having a circuit element (15) on a rear surface, wherein said surface of said first film substrate (12) is opposite to a surface of said second film substrate (10)

and these two film substrates are mutually electrically connected via through holes (46,47) and said first film substrate (12) and said second film substrate (10) are laminated and mutually electrically connected, and they are molded with resin (8).

10. The semiconductor device of claim 8 or 9, wherein said first film substrate (12) is harder than said second film substrate (10).

11. The semiconductor device of claim 9, further comprising an electromagnetic shielding layer (25c) disposed on said surface of said second film substrate (10) for electromagnetically separating said second film substrate (10) from said first film substrate (12).

12. The semiconductor device of claim 9, further comprising a circuit element (23), which is formed on said rear surface of said second film substrate (10) and covered with a material (7) having a dielectric constant lower than that of said resin (8).

13. The semiconductor device of claim 1, wherein said semiconductor chip (2) is covered with a material (7) having a dielectric constant lower than that of said resin (8).

14. The semiconductor device of claim 3, wherein said

semiconductor chip (2) is covered with a material (7) having a dielectric constant lower than that of said resin (8).

15. The semiconductor device of claim 5, wherein said semiconductor chip (2) is covered with a material (7) having a dielectric constant lower than that of said resin (8).

16. The semiconductor device of claim 8 or 9, wherein said semiconductor chip (2) is covered with a material (7) having a dielectric constant lower than that of said resin (8).

17. A semiconductor device substantially as hereinbefore described with reference to the five embodiments illustrated in Figures 1 to 15 of the accompanying drawings.

Examiner's report to the Comptroller under Section 17 (The Search Report)

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Relevant Technical fields

(i) UK Cl (Edition L) H1K (KPF,KPX,KRC,KRD)
H1R (RAV,RBF,RBJ,RBV)

(ii) Int Cl (Edition 5) H01L, H05K

Search Examiner

R C HRADSKY

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search

28 MAY 1993

Documents considered relevant following a search in respect of claims 1-20

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
X	GB 744628 (SPECIALITIES) whole document	1,3,4,7, 10
X	GB 743717 (BDR LTD) whole document	1,4,7,10
X	WO 82/04161 A1 (KONAMI) see Abstract	1,4,7,10
X	EP 0389826 A1 (SEIKO EPSON) see Figure 2	10

Categories of documents

X: Document indicating lack of novelty or of inventive step.

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